

**Los Angeles Valley College
Student Learning Outcomes Assessment Cycle Report
Courses and Programs**

Discipline: Electronics	Department: Technology
Program/Course: Electronics 2 (EL-2)	Semester/Year: Spring 2008
SLO Representative: Ronald Reis	Department Chair: Ronald Reis

Student Learning Outcome Assessed	Students will be able to construct a working circuit from a schematic drawing.
Description of Assessment Method	<p>In assessing whether students in the EL-2 evening class met the student learning outcome stated above, the following measures were used:</p> <ol style="list-style-type: none"> 1. A standard written "matching" test was given, whereby students were asked to identify the schematic symbols for 12 commonly used electronic components. 2. Using solderless circuit board, students were judged as to whether they could accurately connect resistors in series and parallel. 3. Using a DMM (Digital Multimeter), students were asked to accurately measure the resistance of ten randomly chosen resistors. 4. Using a DMM, students were asked to accurately measure the voltage output of a

	<p>randomly chosen set of DC voltages taken from a variable power supply.</p> <p>5. Using a DMM, students were asked to accurately measure the current output from five DC circuits taken from a variable power supply.</p> <p>6. Students were asked to prepare an accurate "Troubleshooting Tree" for the circuit they chose to build.</p>
<p>Assessment Results</p>	<p>Using a direct ten-point scale, where numerical values were calculated in percent, students performed as follows on the six assessment methods addressed above:</p> <ol style="list-style-type: none"> 1. Average score: 90%. 2. Average score: 72%. 3. Average score: 90%. 4. Average score: 85%. 5. Average score: 80%. 6. Average score: 45%. <p>Total average percentage: 77%.</p>
<p>How Results Were Used for Course/Program Improvement</p>	<p>1. While the overall success in constructing an electronic circuit from a schematic drawing was reasonable (77%), clearly students had trouble with preparing an accurate "Troubleshooting Tree" for the circuit they had constructed. More time needs to be spent on "Troubleshooting Tree" design, with more examples given and more design exercises performed.</p>